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Beam-Lead Technology

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A process has been developed to batch-fabricate beam-lead transistors, integrated circuits, and other components, where the leads serve a structural and protective as well as electrical function. Platinum silicide ohmic contacts, titanium and platinum sputtered layers, and electroformed gold beam leads constitute the metallurgical structure of the devices described. Test transistors have survived 350°C aging for hundreds of hours in corrosive ambients, and centrifuging at 135,000 g's.

I. INTRODUCTION

This paper describes a process developed to batch-fabricate semiconductor devices and integrated circuits with electroformed electrodes cantilevered beyond the edges of the wafer — hence, the name beam leads.[1] This type of structure simplifies the assembly and interconnection of individual units and integrated circuits, provides its own protective seal, and leads to a new class of integrated circuits[2] where the isolation is accomplished by etched trenches under the metal bridging connections.

Fig. 1 is a drawing of a silicon high-frequency beam-lead transistor. The 0.5-mil thick leads are cantilevered beyond the edge of the silicon chip, and are used for structural support of the chip as well as electrical contact. The beam leads may be bonded to a metal-filmed substrate with a matching pattern, obviating the need for eutectic brazing to the substrate. This structure imposes no electrical penalty on the

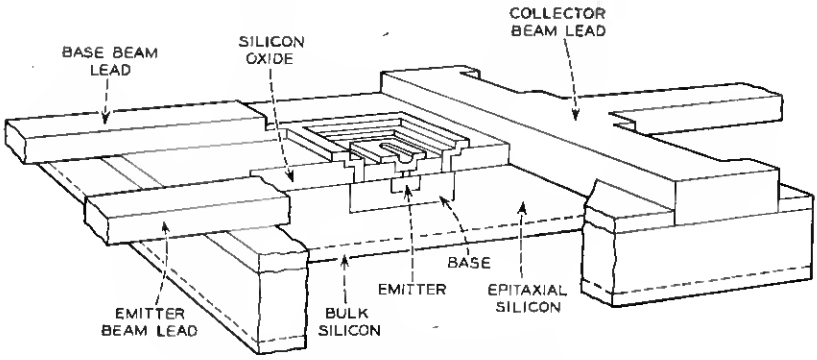

Fig. 1 — Beam-lead transistor structure.

device, the parasitic capacitance being at most equivalent to a conventional planar device.

Fig. 2 is a photo of an actual transistor bonded onto a metallized ceramic substrate. The diffused regions are facing the ceramic.

It can be seen that there are no external wires or brazed areas, as previously mentioned. This device structure has been centrifuged, without failure, to an acceleration level of over 135,000 g's on a test substrate.

Fig. 3 is a photograph of an array of transistors on a slice. There are three different electrode geometries which are used in conjunction with aging experiments. The spacing is approximately 15 mils center-to-center, with every other row missing to allow for test patterns. This spacing leads to a significantly higher packing density than is practical with standard scribe-and-break techniques.

Fig. 4 is a face-view photograph of a beam-lead transistor. The silicon chip is approximately 7-mils square, and the beam leads 1-mil wide. There is an approximate 0.2-mil clearance between the electrode fingers, which are thinner than the beam leads. Thus, the fingers can have the close spacing required for high-frequency operation without carrying the restriction imposed by the required beam thickness.

Basically, the process to be described starts with a standard slice of planar devices after the contact holes have been etched through the oxide. Platinum silicide ohmic contacts are formed in the contact holes; titanium and platinum layers are sputtered onto the silicon oxide; and the gold beam leads are electroformed, using the platinum layer as a base. The excess platinum outside the gold patterns is removed by glow-discharge etching, and the titanium is etched away. At this point, the

Fig. 2 — Bonded beam-lead transistor.

slice is turned over and etch-masking patterns developed in registry with the metallized patterns on the other side. The unmasked areas are etched away, leaving the individual devices with the beam leads cantilevered beyond the edges of the slice.

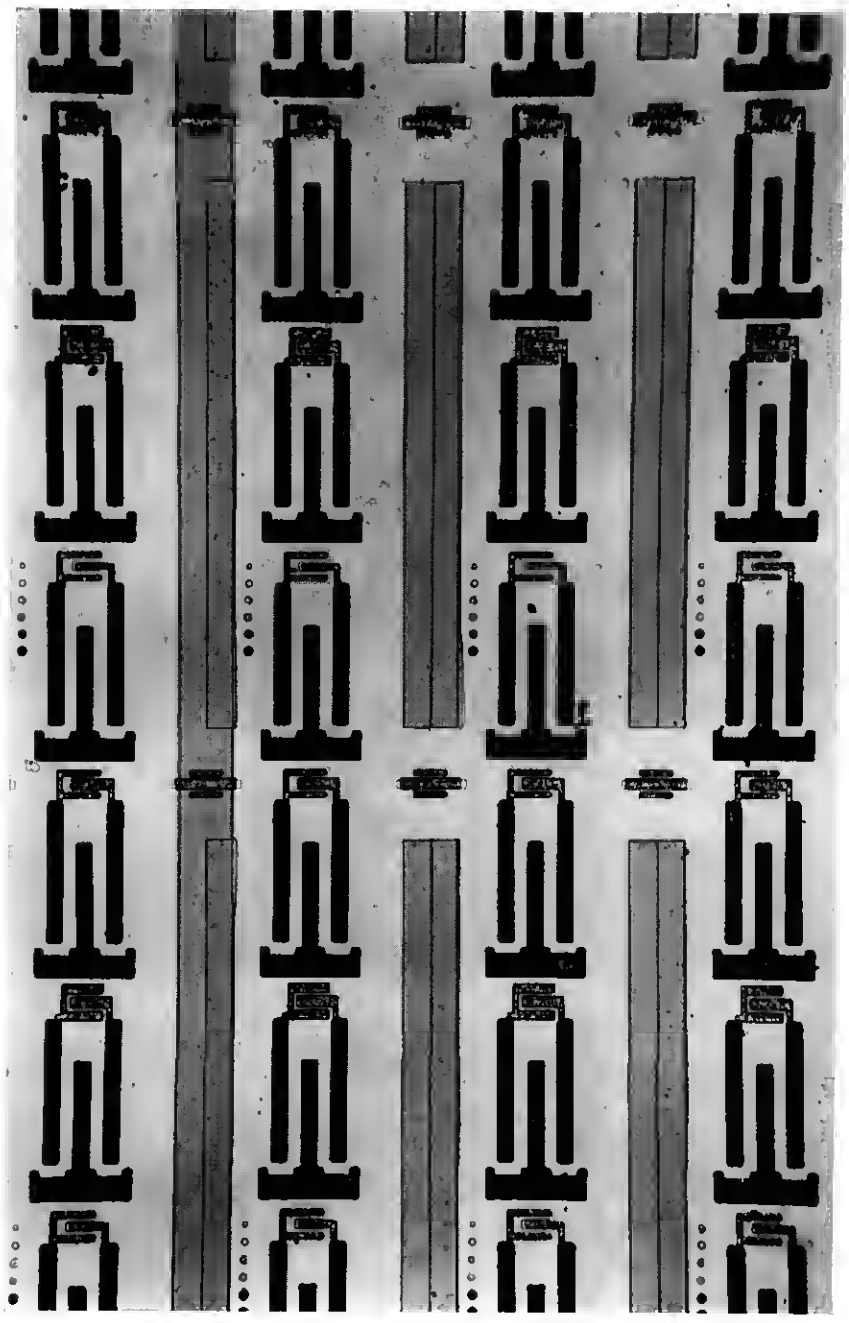

Fig. 3 — Array of transistors.

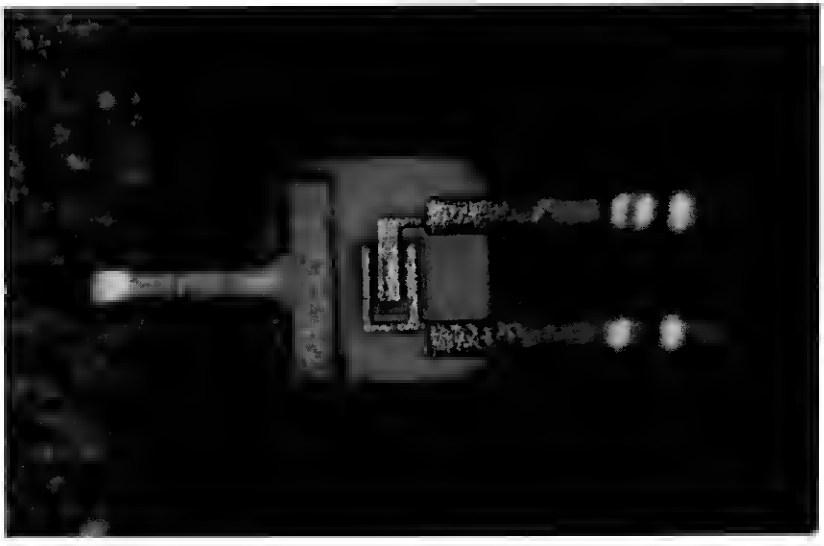

Fig. 4 — Face-view of transistor.

With no additional processing, the previous etching operation may be used to cut isolation trenches in integrated circuits, replacing isolation diffusions or solid-dielectric isolation.

The objective of this project was to produce a semiconductor device structure that would improve the present methods of device assembly, decrease fabrication complexity, yield electrical parameter stability without requiring a separate vacuum-tight enclosure, and decrease integrated circuit parasitic capacitance.

In Section II the beam-lead structure and its applications are discussed; Section III describes a process sequence developed to fabricate devices and integrated circuits; and Section IV is devoted to test results on devices fabricated with the techniques described in Section III.

II. BEAM-LEAD STRUCTURE AND APPLICATIONS

2.1 *Structure*

The beam-lead structure eliminates the need for chip brazing and external wire bonding. With the beam-lead device facing the substrate, the cantilevered leads extending beyond the edges of the chip are

readily aligned with matching patterns on the substrate, and the beam leads bonded to these patterns. The beam leads are used as the alignment guide: with multiple leads extending beyond the chip locating one lead automatically registers the rest, since both the beam-lead array and the substrate pattern are precisely oriented with respect to each other during the photolithographic operations. The surfaces to be joined to each other are both annealed gold, and thermocompression bonding or split-tip welding, among otber techniques, may be used. A gold-gold bond is a very reliable metallurgical system; there are no oxide films to hinder the bonding, gold is one of the most ductile metals, thermocompression bonding occurs at low temperatures (300°C), and the joint formed is free of attack by oxidation, galvanic corrosion, or other corrosive media.

An extension of the beam-lead concept to multiple devices is shown by Fig. 5, a photograph of a string of beam-lead transistors fabricated with common rails connecting all the collectors in a row. This method allows devices to be simply handled in large numbers for feeding, electrical testing, and bonding. As required, one device is bonded to a substrate, and broken from the string. Since the string is initially fabricated as an array on the silicon slice, all dimensions are held to close tolerances, and any lead is precisely oriented with respect to any other point in the string, typically within 0.1 mil. In addition, tbe device need never be handled by the silicon chip. The gold leads and supporting ribs absorb the handling stresses and possible contamination.

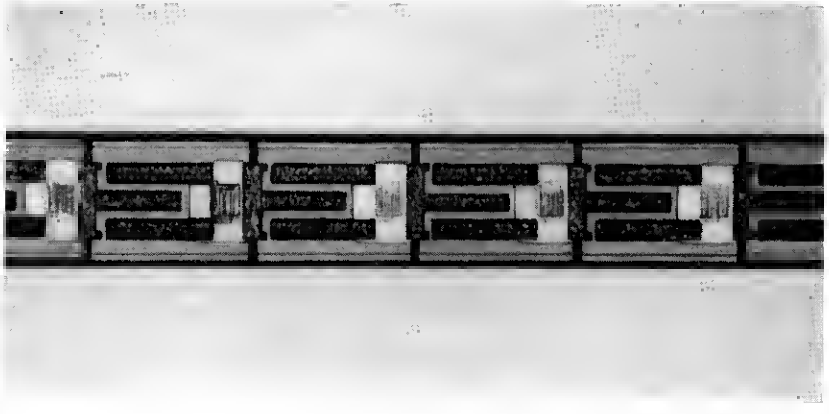

Fig. 5 — String of transistors.

2.2 *Applications*

An early application of beam-lead transistors to discrete-chip integrated circuits is seen in Fig. 6, which is a photograph of two DCTL gates with three and four inputs. There are seven high-frequency silicon transistors (3 leads), and nine beam-lead boron-diffused silicon resistors. Several circuits wired as a 3-stage ring oscillator, with a fan-in of 3-4, and a fan-out of 1, yielded a measured propagation delay of 4.2

Fig. 6 — Discrete-chip integrated circuit.

ns. Measurements were made with a collector supply voltage of 5 volts, corresponding to an average power per gate of 23 mw. This is equivalent in performance to circuits fabricated with standard chip and wire construction.

Fig. 7 is an example of beam-lead transistors appliqued to a tantalum thin-film circuit, a 3-2 input gate DCTL switching circuit. With this structure, it is not necessary to braze the silicon chips to the substrate, subjecting precise resistors to the bonding temperature required for eutectic brazing. Ultrasonic or split-tip resistance welding may be employed to attach the beam-lead devices to the metallized

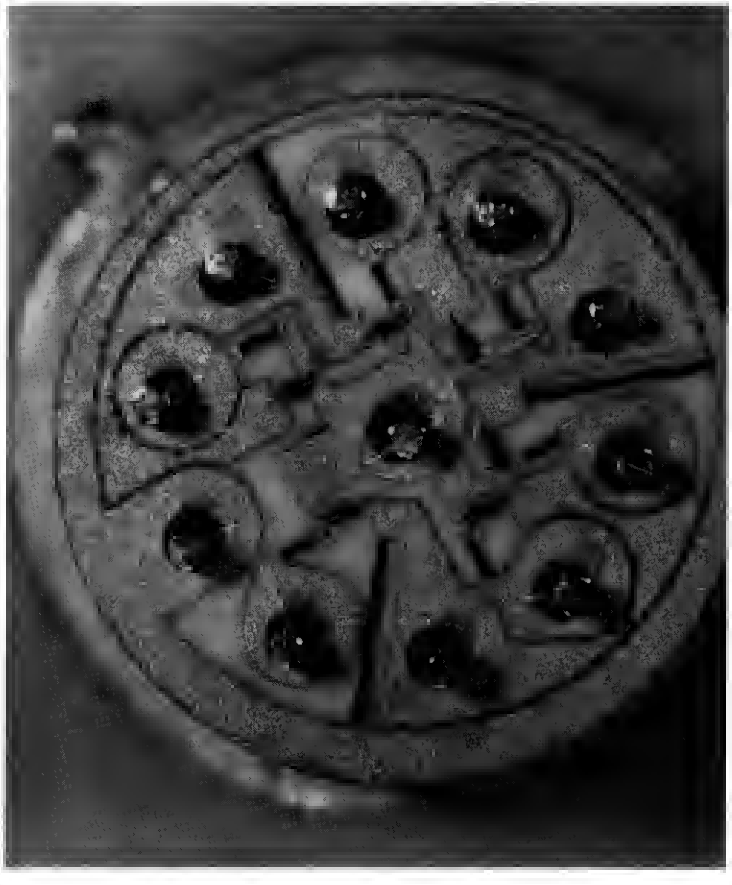

Fig. 7 — Hybrid thin-film digital circuit.

substrate. A TO-5 header and pin-connecting wires are used in this circuit for convenience only.

A specific application of beam-lead techniques to monolithic integrated circuits was investigated by H. A. Waggener.[2] As a consequence of etching away the unwanted silicon from under the beam leads, isolated pads of silicon may be attained, interconnected by the beam leads. The only capacitive coupling is then through the small metal-over-oxide overlay (0.05 pf typical). This is many times lower than the junction capacitance incurred with p-n junction isolation monolithic circuits. Ultrahigh-speed switching circuits are possible with this technique, with no increase in processing complexity. The isolation trenches are automatically formed during the silicon etching.

Fig. 8 is a physical-electrical schematic of a 4-input DCTL logic gate. This circuit was chosen because of its common occurrence, and sufficient complexity to illustrate "beam-lead" (isolation) techniques.

Electrical measurements of switching performance were performed

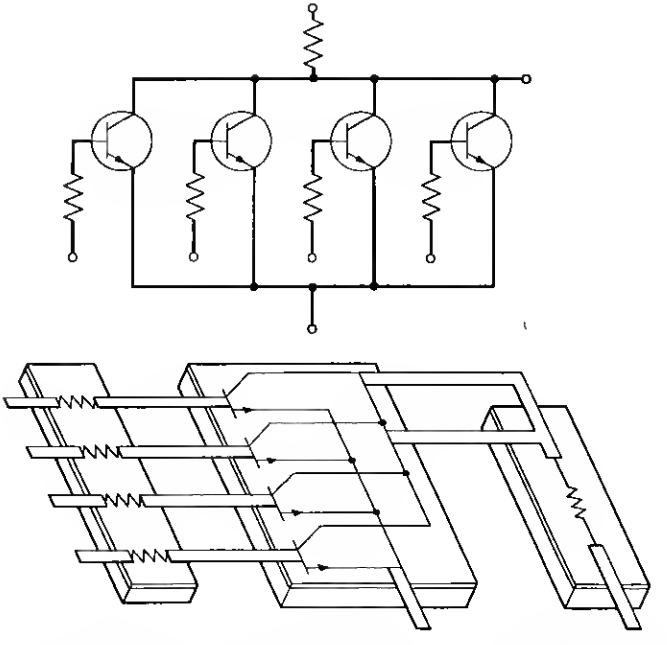

Fig. 8 — Circuit schematic of DCTL gate and physical-electrical schematic showing component placement.

on 3-stage ring oscillators. Propagation delays of 4 ns were obtained, equivalent to the switching speed of comparable discrete device circuits. More complex circuits are currently under development.[3]

Figs. 9 through 11 are examples of beam-lead integrated circuits.

III. BEAM-LEAD PROCESSING

3.1 *Contact System*

Beam leads can be fabricated using many different metallurgical combinations, depending upon the environmental and thermal conditions the device must withstand. The objective of this project was to produce a contact structure for silicon devices that would survive 350°C oxidizing ambients, steam or air, continuously for 1000 hours without degradation. The metallurgical system Pt_5Si_2-Ti-Pt-Au was chosen, and the techniques developed to produce this structure are described in the following paragraphs.

The starting material is a slice of standard planar-oxidized silicon devices with contact holes etched in the SiO_2. At this stage the device

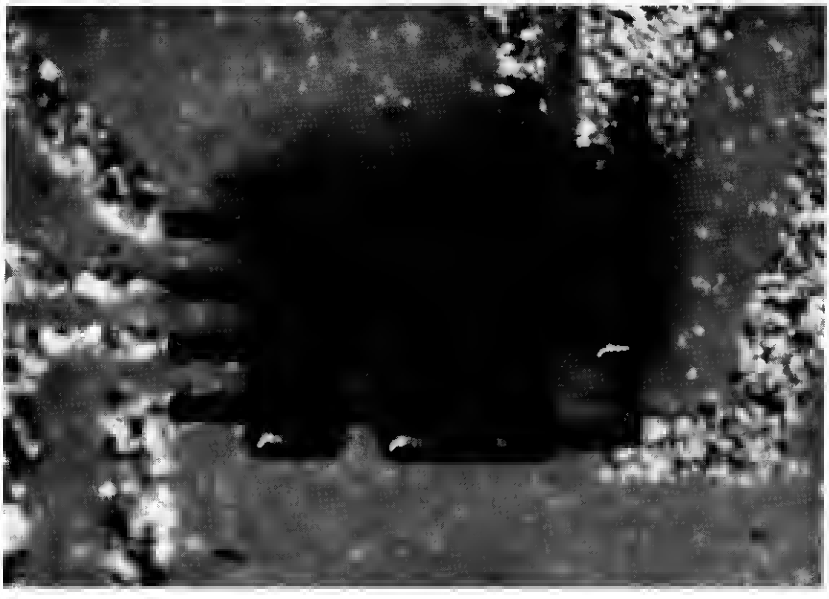

Fig. 9 — Beam-lead integrated DCTL gate mounted on gold-metallized ceramic, device side down.

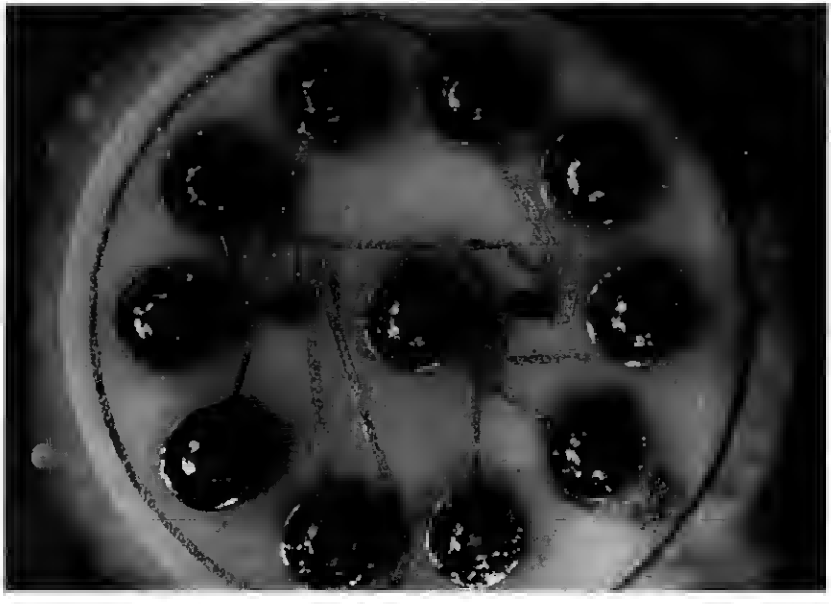

Fig. 10 — Two beam-lead integrated DCTL gates mounted on TO-5 header.

is ready for ohmic contacts. Platinum silicide was chosen as the ohmic contact material. It is one of the most stable compounds of silicon, has extreme corrosion resistance, is a solid phase up to 980°C,[4] has an optical reflectivity different from either silicon or platinum, and forms an ohmic contact to heavily-doped silicon. To form the compound in the contact holes, platinum is sputtered onto the whole slice after the contact holes are opened in the oxide, and heated to 700°C while still in the inert atmosphere. The platinum in the holes will react with the silicon to form Pt_2Si, which is a solid phase and will not ball up or creep beyond the edges of the contact holes as a liquid eutectic would. In addition, the silicide is a different color from platinum and can readily be distinguished from it under a microscope. Fig. 12 is a photograph of a device with the silicide formed in the contact hole. With improperly etched contact holes, spotty silicide formation or even no silicide at all is observed. An example of improper reaction is shown in Fig. 13. This is a photo of an integrated circuit. The square area with 3 contact stripes is a diffused base area; the two outside stripes are base contact stripes, and the center stripe is an emitter contact stripe. It can be seen that one of the base fingers in two different tran-

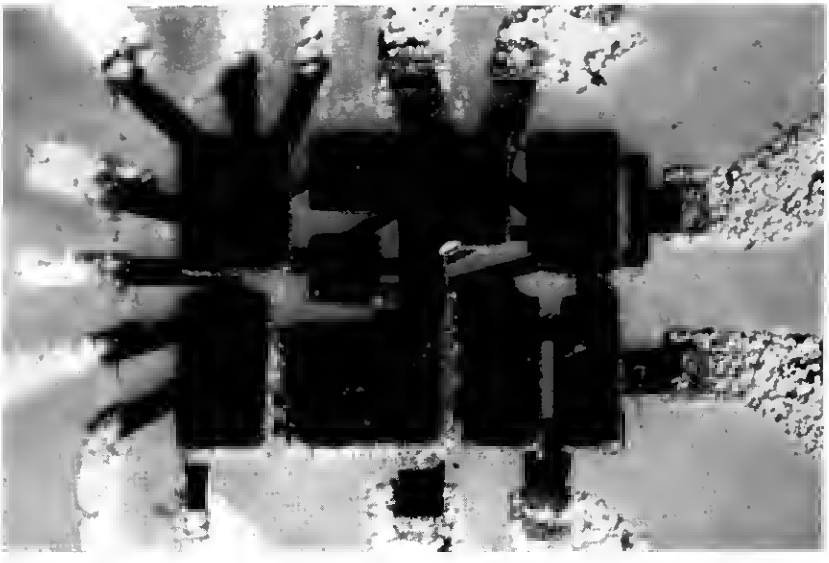

Fig. 11 — Dual 4-input DTL gate mounted on gold-metallized substrate, 0.030 inch over-all.

sistors has not formed the silicide; these two devices will not show proper electrical performance due to emission from only one edge of the emitter. This reason for substandard electrical characteristics would not have been detected if standard contacts had been used.

After the visual inspection, the platinum that is over the oxide is removed, leaving the silicide in the contact holes.

The next operation is to apply a material that will bond to both the SiO_2 and the Pt_5Si_2 and serve an an electrical connection to the external circuitry. No single element will satisfy all these conditions; however, a composite layered structure consisting of Ti-Pt-Au has been successfully employed. The first layer, titanium, is chosen because of its high oxygen activity, refractory nature, ability to absorb almost half its weight in reaction products interstitially[5] (commonly called "gettering"), and the natural oxide that it does form is completely self-passivating at temperatures up to 400°C. Although other metals, such as zirconium and hafnium, would probably be adequate, successful prior experience with titanium active metal semiconductor contacts[6] on such devices as shallow-junction solar cells for communications satellites and high-frequency silicon transistors makes titanium a logical choice for the oxide-bonding layer.

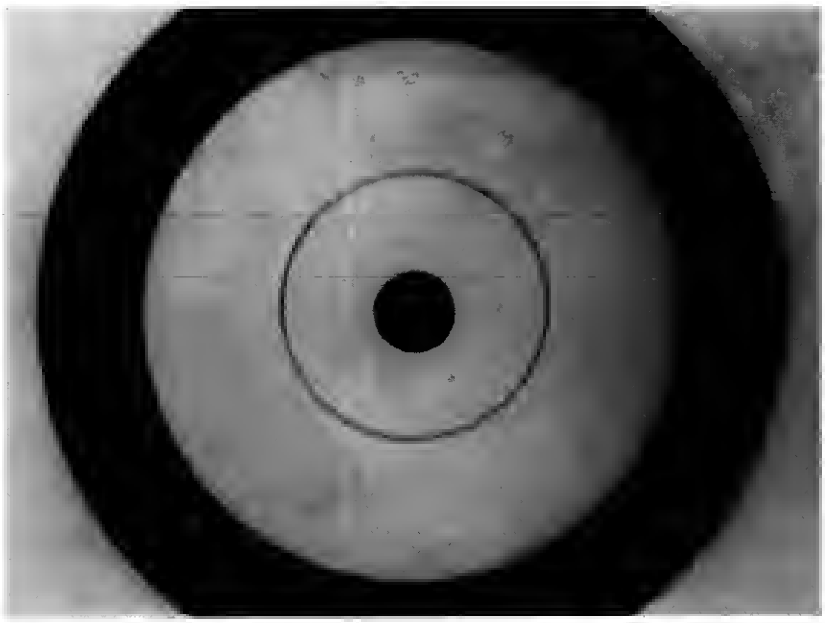

Fig. 12 — Platinum silicide ring-dot contact.

Table I is a list of some common metals, and the free energies of formation of their oxides,[7] in order of activity. This list may be used as a guide to the surface-bonding strengths. Titanium is the first active metal after silicon, and in addition to its great surface bonding strength may be used to penetrate thin SiO_2 layers. This property presumably allows titanium films to getter impurities from the passivating SiO_2 layer.

Gold is chosen as the outer layer because of its extreme resistance to corrosion, ease of bonding, low yield point, high elongation (allowing thermal expansion mismatch with the silicon substrate), and suitability for high-resolution electroforming. However, gold is a metallurgically reactive material, and reacts with titanium chemically at relatively low temperatures to form compounds which have none of the desirable characteristics of the individual metals. This leads to the third metal in the sandwich; platinum is chosen as the filler because of its inertness, ease of bonding the gold outer layer, and the low diffusion coefficient of gold into platinum (D less than 10^{-10} cm^2/sec at 900°C).[8]

Fig. 13 — Improperly reacted contact holes.

3.2 *Sputtering*

Metal films are normally deposited onto semiconductors by vacuum evaporation. The use of the electrodes in beam-lead devices as structural supports, however, requires extreme adherence of the titanium to the SiO_2 layer. With the many processing operations and handling steps in producing a planar device, the surface cleanliness is variable from slice to slice. Since sputtered metals have many times the energy of thermally evaporated metals, and are capable of dislodging impurities, it was decided to use this method for the application of the titanium and platinum layers. The sputtering apparatus is shown in Fig. 14.

3.3 *Electroforming*

The method chosen to deposit the 0.5-mil thick gold beam leads is electroforming, the build-up of material by electroplating in selective areas. This technique has been developed to the point where extremely

TABLE I — FREE ENERGY OF FORMATION OF METAL OXIDES AT 500°K IN ORDER OF ACTIVITY

Oxide	$-F^\circ$ (Kcal/mole)	$-F^\circ$ (Kcal/gram atom oxygen)
NiO	46.1	46.1
MoO_2	114.5	57.2
Cr_2O_3	240.2	80.1
Na_2O	83.0	83.0
Ta_2O_5	434.9	87.0
SiO_2	187.9	94.0
TiO	112.2	112.2
ZrO_2	238.4	119.2
Al_2O_3	362.1	120.7

small geometries are feasible. Using high resolution KPR, dimensions under 0.2 mil are possible. Fig. 4 is a photograph of a high-frequency transistor with electroformed beam leads. The electrode fingers are plated to a thickness of 0.2 mil, thinner than the 0.5-mil thick beam leads, allowing the close spacing necessary for high-frequency operation. The aspect ratio of the fingers (height/width) can approach one for thin fingers.

3.4 *Back-Sputtering*

At this stage the electrodes and beams are defined by the gold. The remainder of the slice is coated with continuous layers of titanium and platinum, and patterns of gold beam leads and electrode fingers. Removing the platinum and titanium, in this order, from the areas outside the gold patterns remains to complete the metallizing process. Titanium is easily etched using the gold patterns as etch masks; however, platinum is much more difficult to etch than gold, especially without undercutting the narrow gold fingers. Therefore, a technique has been developed whereby the platinum is etched by glow discharge bombardment, now called "back-sputtering".

Fig. 15 is a drawing of the apparatus used for back-sputtering. A slice of oxidized and metallized silicon, up to one inch in diameter, is placed upon a ceramic spacer which is placed upon an aluminum cathode, and a glow discharge is excited with the cathode at -5 kv. The oxide thickness on the silicon slice is under 1 micron thick, and if this voltage appeared across the oxide, the dielectric stress would be 5×10^7 volts/cm, which is greater than the breakdown strength of the oxide. For thinner oxides, the stress would be correspondingly higher.

Fig. 14 — Sputtering apparatus.

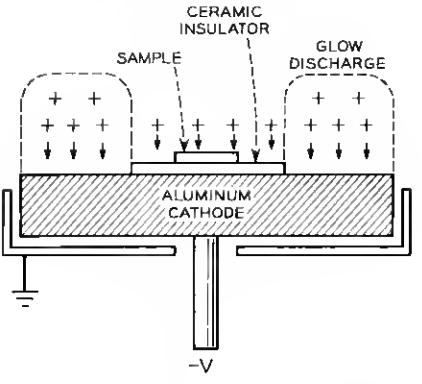

Fig. 15 — Drawing of back-sputtering apparatus.

The purpose of the ceramic spacer is therefore to prevent the dc field from appearing across the passivating oxide on the slice of devices should the metal film, shorting the edge of the slice, erode away.

Patterns of platinum, gold, rhodium, iridium, chrome-platinum, etc. have been delineated using this technique. In addition, holes have been etched into SiO_2 films using aluminum patterns as back-sputtering masks. The holes formed in this manner have very straight-sided edges due to the directional velocity of the bombarding ions. The limit of resolution of this technique is that of the masking procedure employed.

IV. TEST RESULTS

4.1 *Mechanical*

Special fixtures have been built to mechanically test beam-lead devices, and centrifuging has been performed to 135,000 g's without failure. Bending tests performed on the leads by bending over a 2-mil radius have yielded twenty 90° bends before breakage; 1.5-mil gold wire used as a control failed at 17 bends. Devices have also been successfully removed from substrates and reused. This attests to the strength and ductility of the electroformed leads.

Corrosion testing for periods up to 1000 hours in 350°C steam, 350°C air, and 350°C wet NaCl has revealed no physical or electrical deterioration of beam leads. In addition, temperature cycling and galvanic corrosion aging has been equally harmless.

4.2 *Junction Aging*

As a by-product of the metallization procedure described in the preceding section, there is considerable enhancement of surface stability and junction quality. This is attributed to the use of the sputtered Ti, a highly energetic getter-metal. pnp transistors, extremely sensitive to collector channel formation,[10] were fabricated and aged. One group was processed by normal procedure, using evaporated aluminum contacts; these devices acted as controls. Another group was processed with Pt-Ti-Pt-Au contacts, with half the group having junction-overlay contacts, and the other half non-overlay. An overlay contact is defined as a contact where the metal is delineated so that it remains on the oxide surface and extends beyond the junction. The two groups were then aged in 350°C steam. Fig. 16 is a graph of the collector leakage current during aging. The collectors of the control group (aluminum contacts) channeled within two hours, the collector leakage currents reaching hundreds of microamperes. The Ti-Pt contacted devices had leakage currents in the subnanoampere range after 400 hours, at which point the experiment was inadvertently terminated.

The curve of Fig. 17 illustrates the collector reverse current as a function of aging of a typical overlay pnp transistor under 21 volts reverse bias at 220°C. The reverse current, I_{cbo}, rose to 1 na after 50

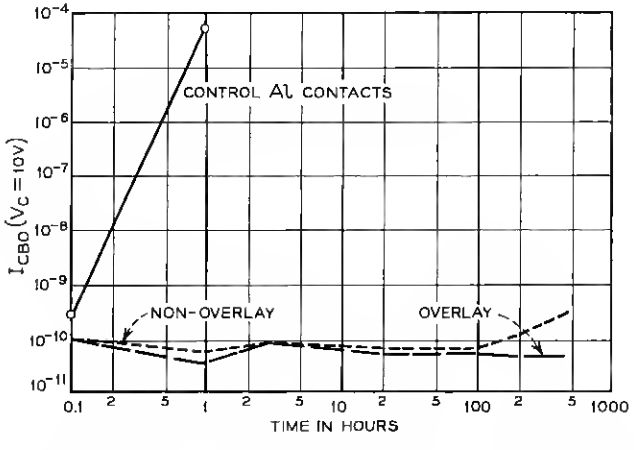

Fig. 16 — Graph of collector reverse current as a function of aging time in 350°C steam.

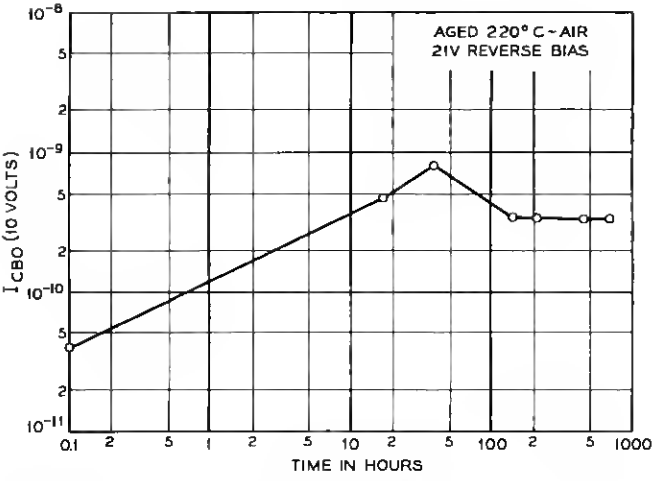

Fig. 17 — Graph of collector reverse current as a function of aging time under 21-volt bias and 220°C air.

hours, and then decayed to an equilibrium value in the 10^{-10} ampere range.

npn transistors, not prone to channel formation, have also been similarly aged, with favorable results for overlay, non-overlay, and completed beam-lead structures.

4.3 *Contact Resistance*

Forward junction characteristics have been monitored during aging in these hot, corrosive atmospheres. Typical resistance changes on contact areas of 0.2 × 1.6 mils are under 0.1 ohm after 1000 hours in 350°C air or steam; this is the measurement resolution. Obviously no "plaguing" problem has arisen with this metallurgical system since films formed at any of the metal interfaces would yield an increase in contact resistance, or require burning-in.

V. CONCLUSIONS

A semiconductor device structure and its application to high-frequency silicon switching transistors and ultrahigh-speed integrated circuits have been described. Beam leads have been shown to be rugged;

units have survived corrosive atmospheres (350°C steam), severe bending, and 135,000 g's centrifuging.

This structure imposes no electrical penalty; parasitic capacitance (under 0.05 pf per lead) is equivalent to wire-bonded and brazed-chip assembly. The beam-lead concept is applicable to many other electronic devices as well. In addition, the electroformed leads are not required to be of constant cross-section. They can taper out as they leave the silicon surface for lower inductance, stripline impedance matching, and even better heat conductance.

Assembly of these devices is considerably simplified. Chip-brazing and wire-bonding are eliminated; devices need not be handled by the silicon chip itself. The feasibility of this structure has been shown in the variety of digital, linear, and thin-film applique circuits which have been fabricated. Multiple arrays are the result of batch-fabrication of devices leading to the possibility of more automatic handling and assembly.

Isolation for integrated circuits is accomplished as a by-product of the structure. Parasitic capacitance has been shown to be negligible, and switching times are comparable to equivalent chip-and-wire circuitry. This has been achieved with no increase in process complexity over discrete devices.

The metallizing procedures developed to fabricate beam-lead devices yield an increase in device reliability; contact resistance is maintained at a low value during stringent accelerated aging tests; and passivation of junctions and surfaces has been enhanced. In addition, glow discharge etching has been developed, allowing the design of photo-reproduced geometries (down to 1 micron) of inert materials such as rhodium and iridium, compatible with normal device processing. Electroformed gold patterns of high resolution are employed as standard procedure.

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Errata

Measurements of Electromagnetic Backscattering from Known, Rough Surfaces, by J. Renau and J. A. Collinson, B.S.T.J., *44*, December, 1965, pp. 2203–2226.

On page 2204, replace the last two lines of the abstract with *an rms slope of 8° ± 4°, and a dielectric constant ε of 1.9 ± 0.3 at microwave frequences.* On page 2221, replace

$$m \equiv \frac{4\pi h}{\lambda} \cos \lambda \gtrsim \frac{1}{10}$$

with

$$m \equiv \frac{4\pi h}{\lambda} \cos \psi \gtrsim \frac{1}{10}.$$

From the experimental evidence presented, the condition on small m, p. 2221, for a surface to appear rough, in a radar sense, should have read $m \gtrsim 1$ instead of $m \gtrsim \frac{1}{10}$.